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PATENT & TRADEMARK OFFICE

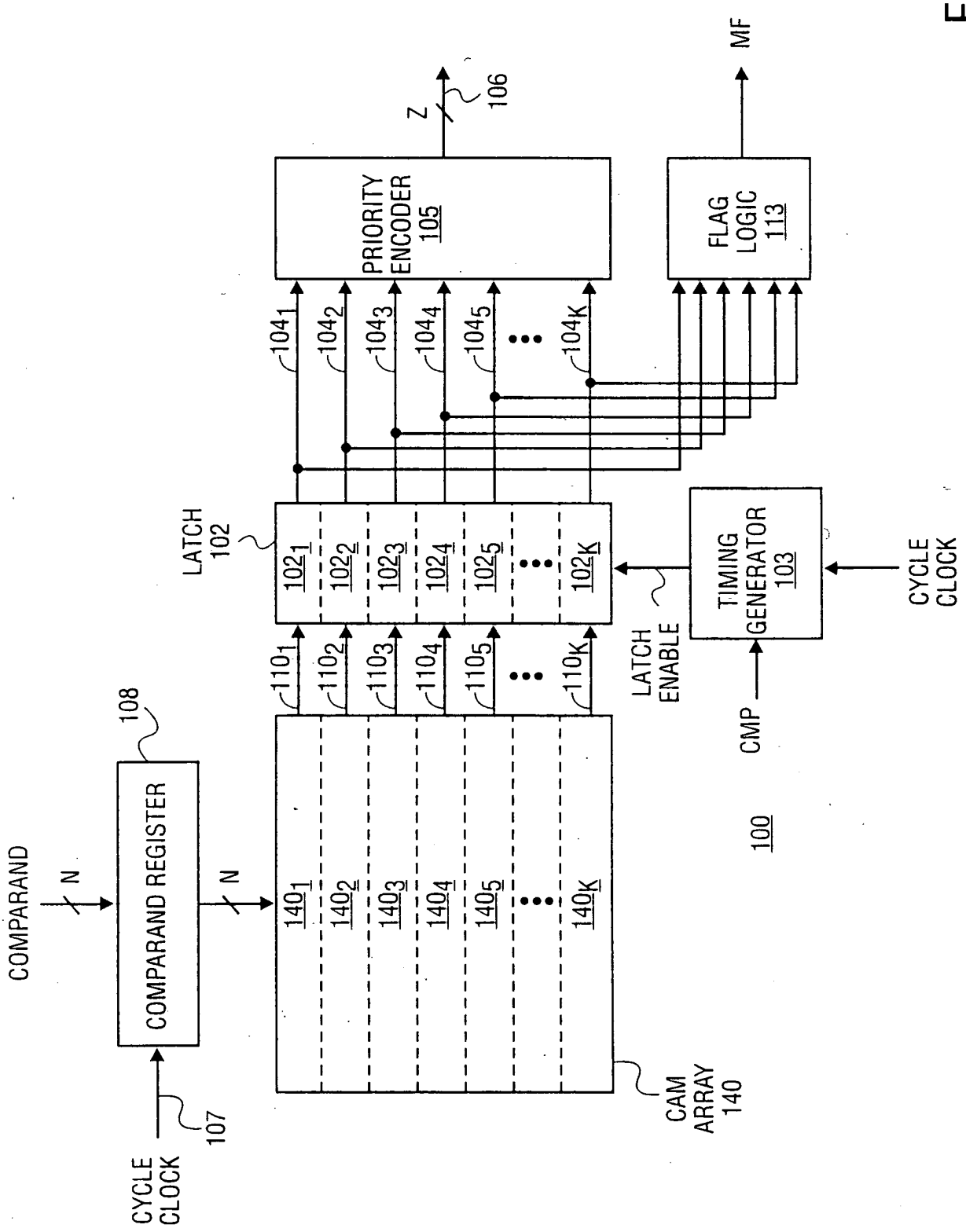

FIG. 1

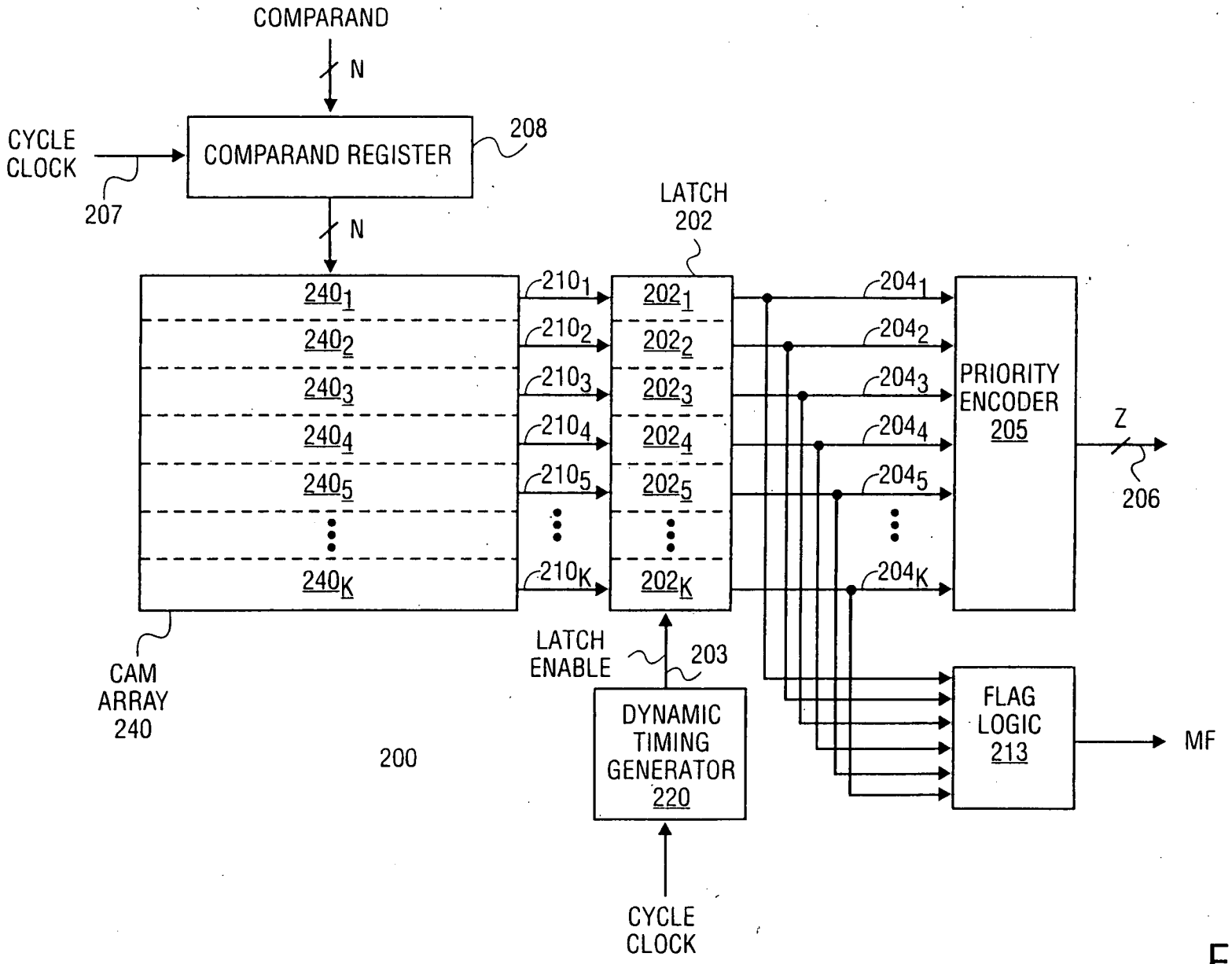
COMPARAND
N
CYCLE CLOCK
COMPARAND REGISTER
208
207
N
LATCH 202
240_1
240_2
240_3
240_4
240_5
240_K
210_1
210_2
210_3
210_4
210_5
210_K
202_1
202_2
202_3
202_4
202_5
202_K
204_1
204_2
204_3
204_4
204_5
204_K
PRIORITY ENCODER 205
Z
206
CAM ARRAY 240
LATCH ENABLE
203
DYNAMIC TIMING GENERATOR 220
FLAG LOGIC 213
MF
200
CYCLE CLOCK

FIG. 2

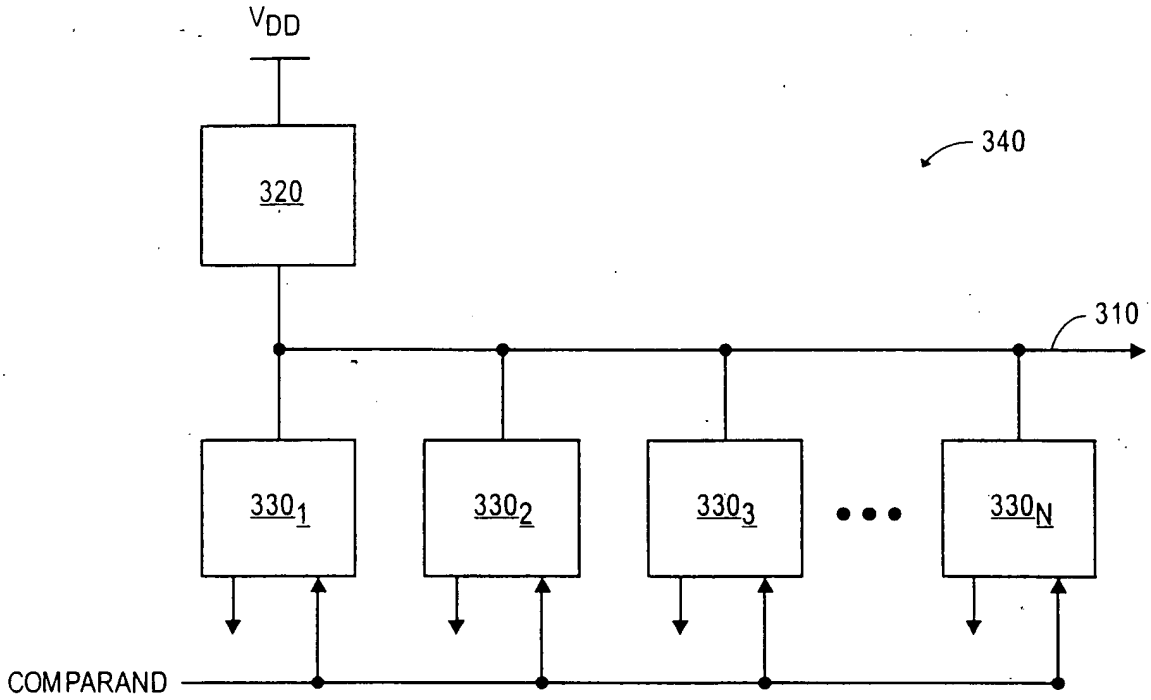
V_{DD}
320
340
310
330_1
330_2
330_3
330_N
COMPARAND

FIG. 3

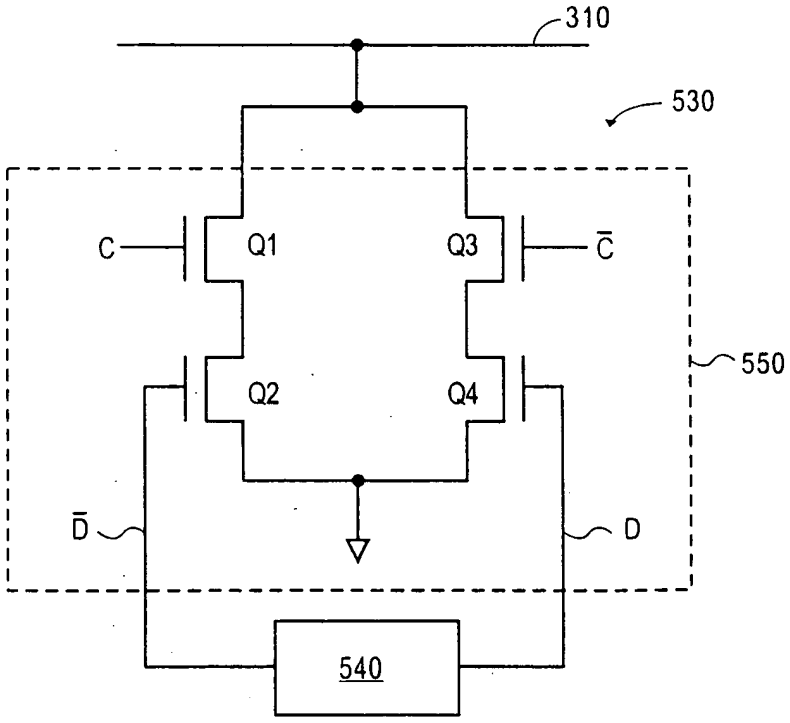
310
530
C
Q1
Q3
$\bar{C}$
Q2
Q4
550
$\bar{D}$
D
540

FIG. 5

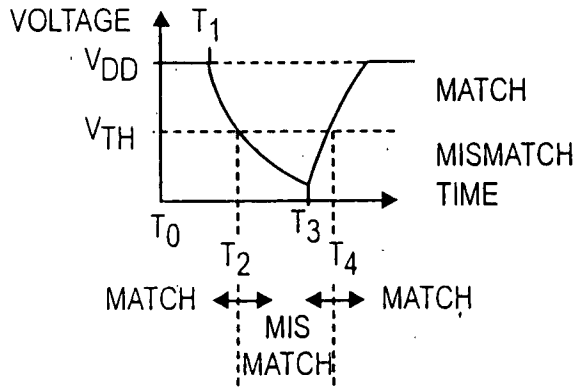
VOLTAGE
T_1
V_{DD}
V_{TH}
MATCH
MISMATCH
TIME
T_0
T_2
T_3
T_4
MATCH
MATCH
MIS
MATCH

FIG. 4

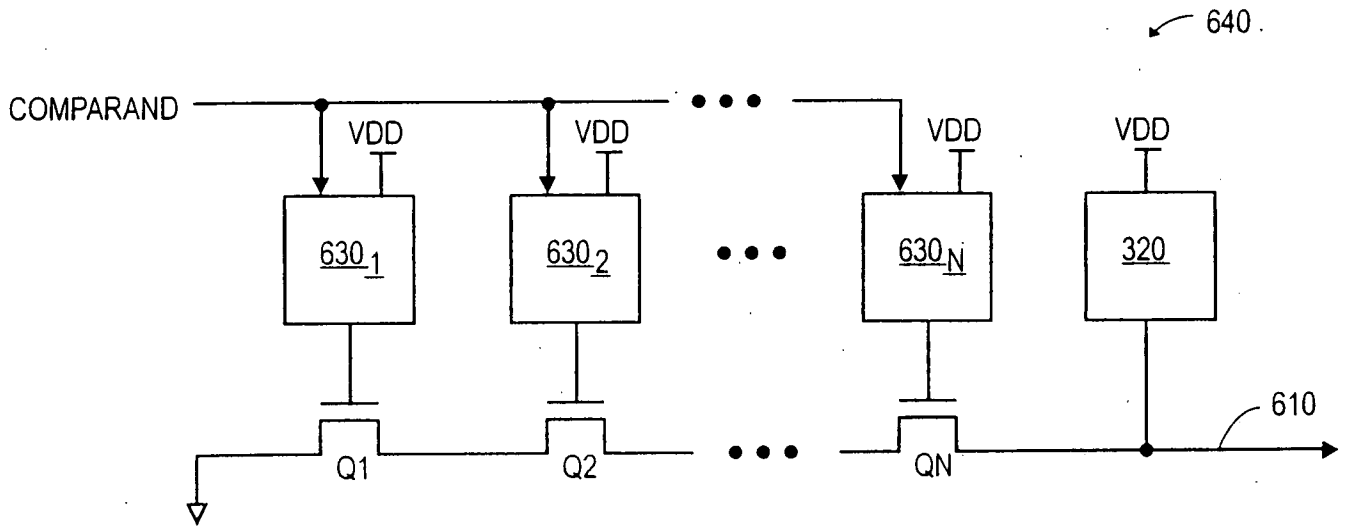
640
COMPARAND
VDD
VDD
VDD
VDD
630_1
630_2
630_N
320
610
Q1
Q2
QN

FIG. 6

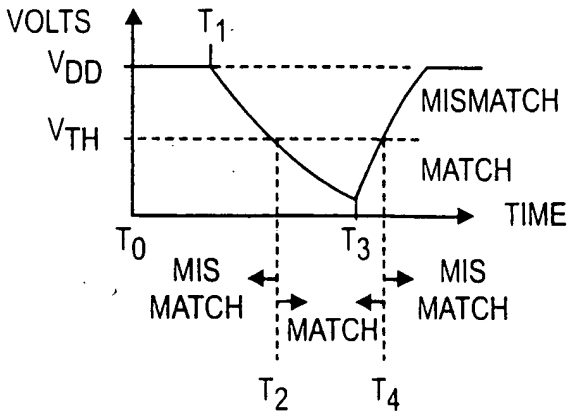
VOLTS
T_1
V_{DD}
V_{TH}
MISMATCH
MATCH
TIME
T_0
T_3
MIS MATCH
MATCH
MIS MATCH
T_2
T_4

FIG. 7

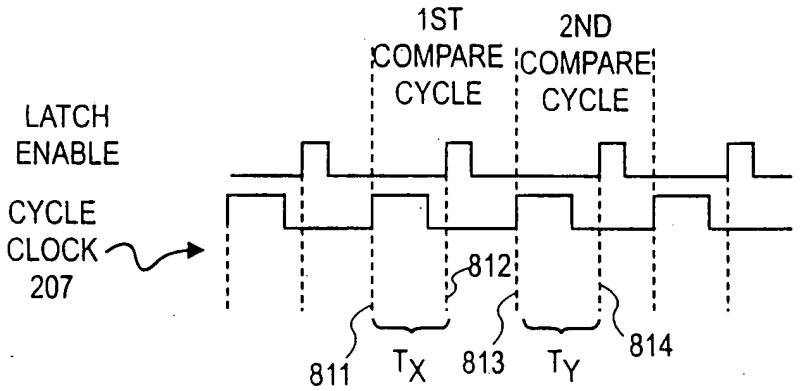
1ST COMPARE CYCLE
2ND COMPARE CYCLE
LATCH ENABLE
CYCLE CLOCK 207
812
811
T_X
813
T_Y
814

FIG. 8

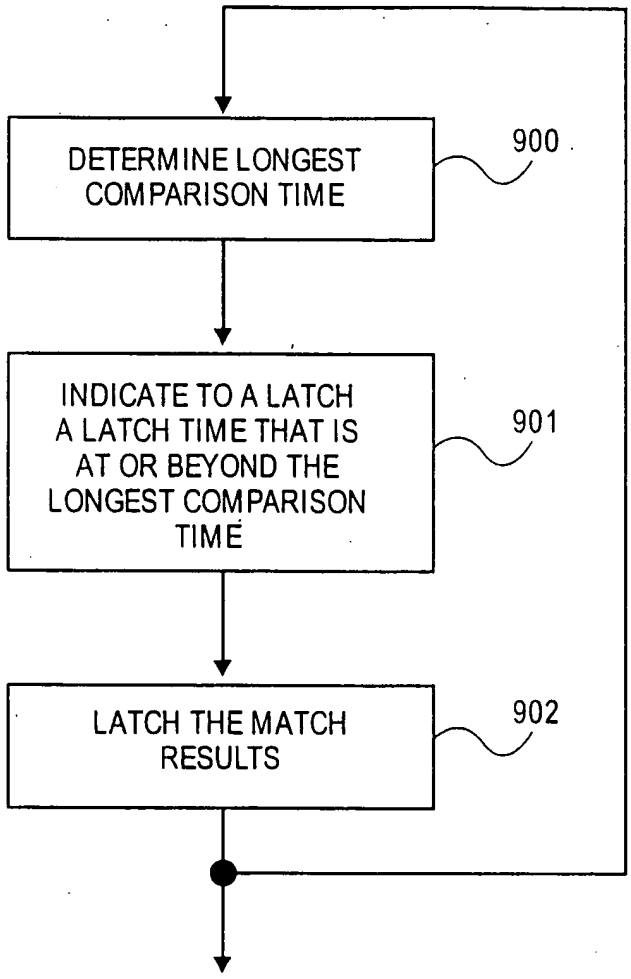
DETERMINE LONGEST COMPARISON TIME
900
INDICATE TO A LATCH A LATCH TIME THAT IS AT OR BEYOND THE LONGEST COMPARISON TIME
901
LATCH THE MATCH RESULTS
902

FIG. 9

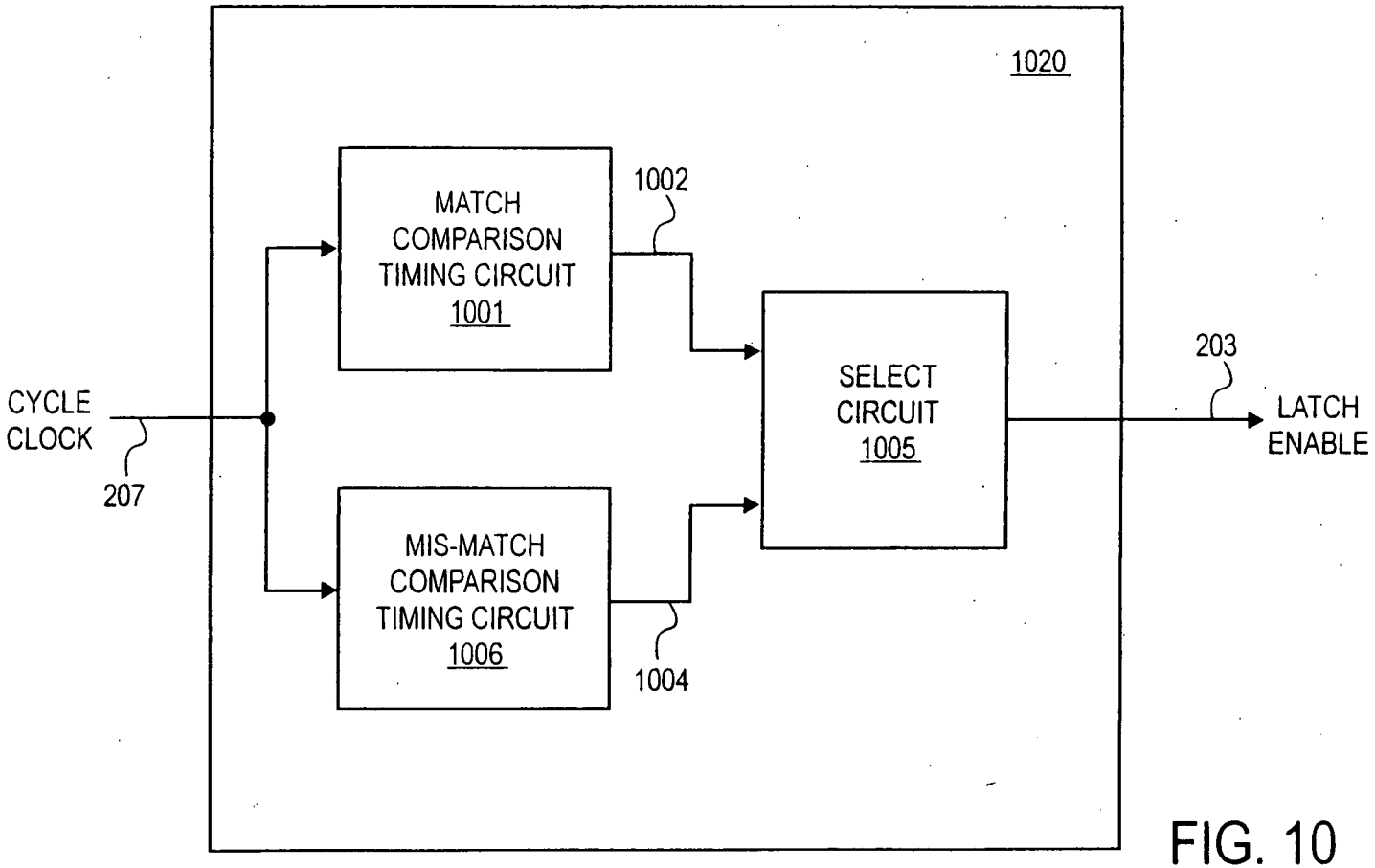
1020
MATCH
COMPARISON
TIMING CIRCUIT
1001
1002
SELECT
CIRCUIT
1005
203
LATCH
ENABLE
CYCLE
CLOCK
207
MIS-MATCH
COMPARISON
TIMING CIRCUIT
1006
1004

FIG. 10

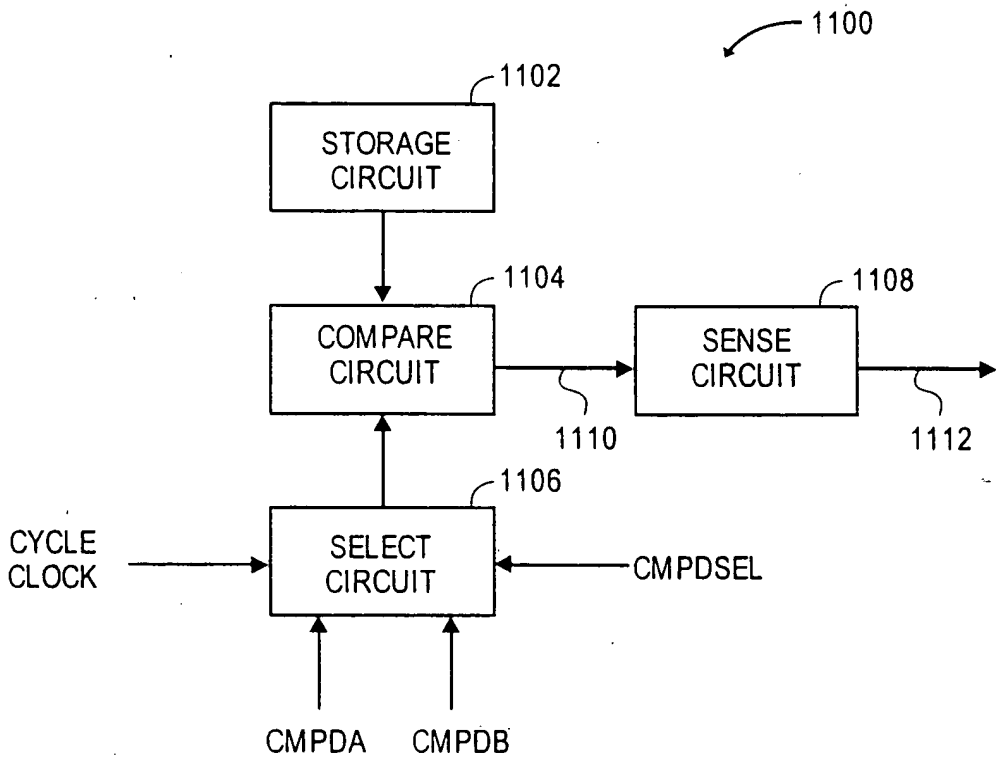
1100
1102
STORAGE CIRCUIT
1104
COMPARE CIRCUIT
1108
SENSE CIRCUIT
1110
1112
1106
CYCLE CLOCK
SELECT CIRCUIT
CMPDSEL
CMPDA
CMPDB

FIG. 11

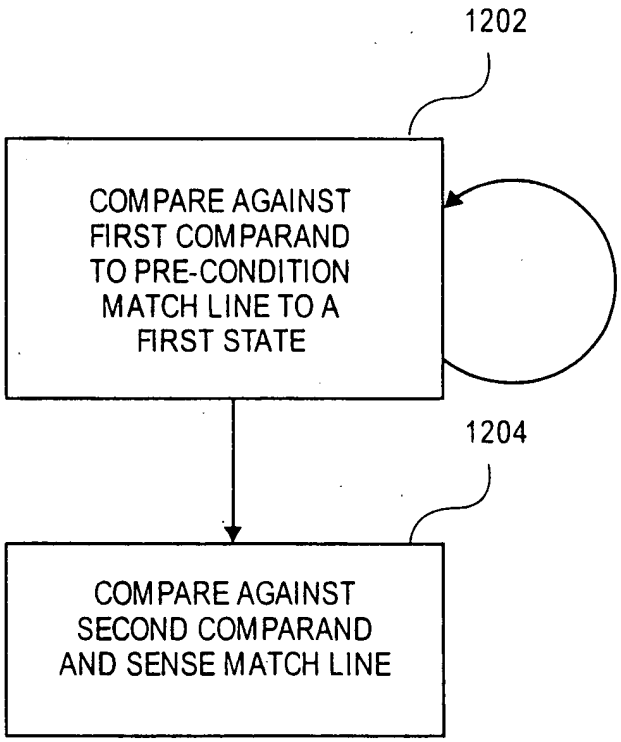
1202
COMPARE AGAINST FIRST COMPARAND TO PRE-CONDITION MATCH LINE TO A FIRST STATE
1204
COMPARE AGAINST SECOND COMPARAND AND SENSE MATCH LINE

FIG. 12

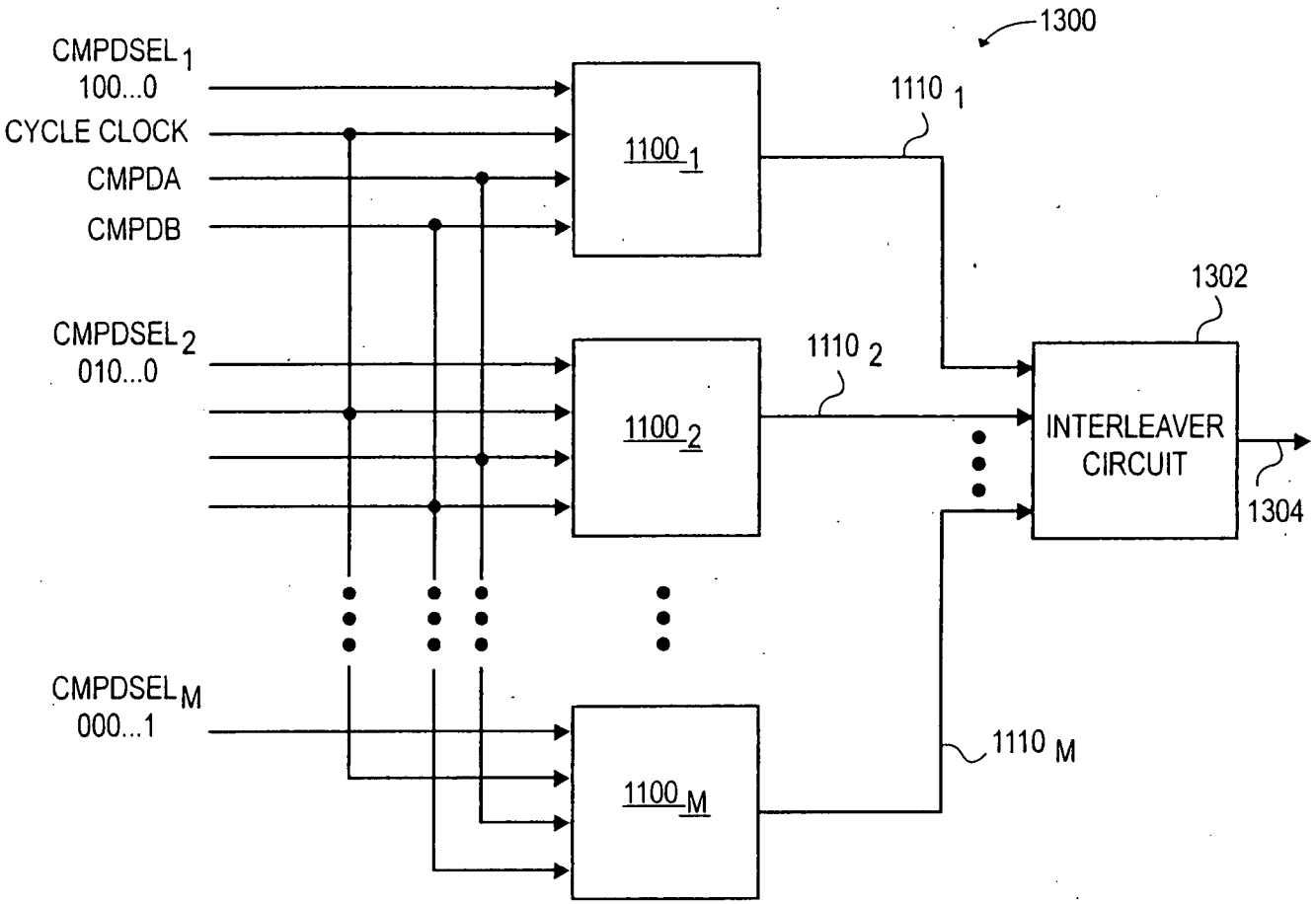
1300
CMPDSEL 1
100...0
CYCLE CLOCK
CMPDA
CMPDB
CMPDSEL 2
010...0
CMPDSEL M
000...1
1100 1
1100 2
1100 M
1110 1
1110 2
1110 M
1302
INTERLEAVER CIRCUIT
1304

FIG. 13

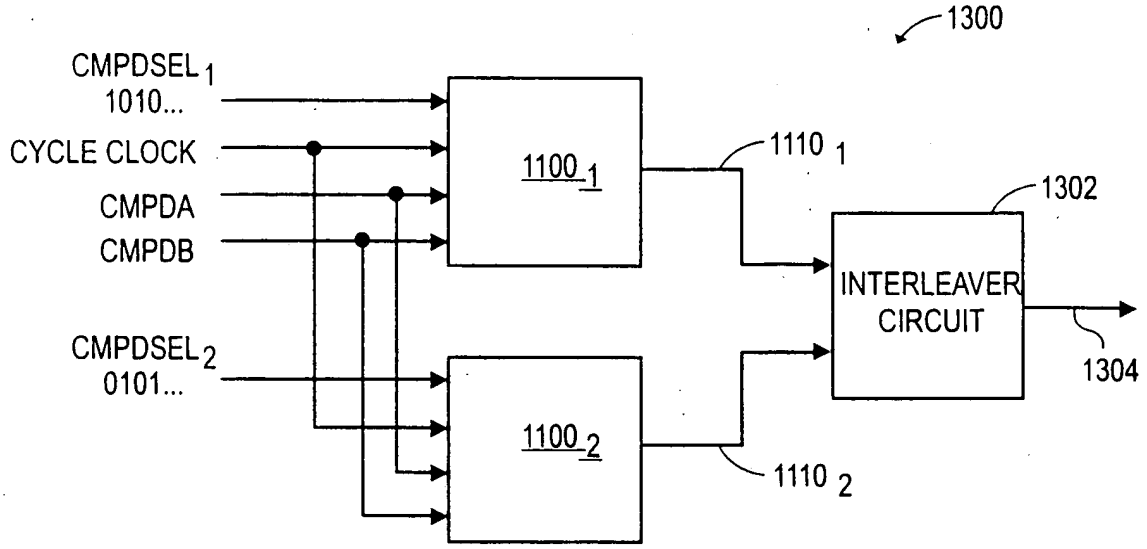
1300
CMPDSEL 1
1010...
CYCLE CLOCK
CMPDA
CMPDB
CMPDSEL 2
0101...
1100 1
1100 2
1110 1
1110 2
1302
INTERLEAVER CIRCUIT
1304

FIG. 14

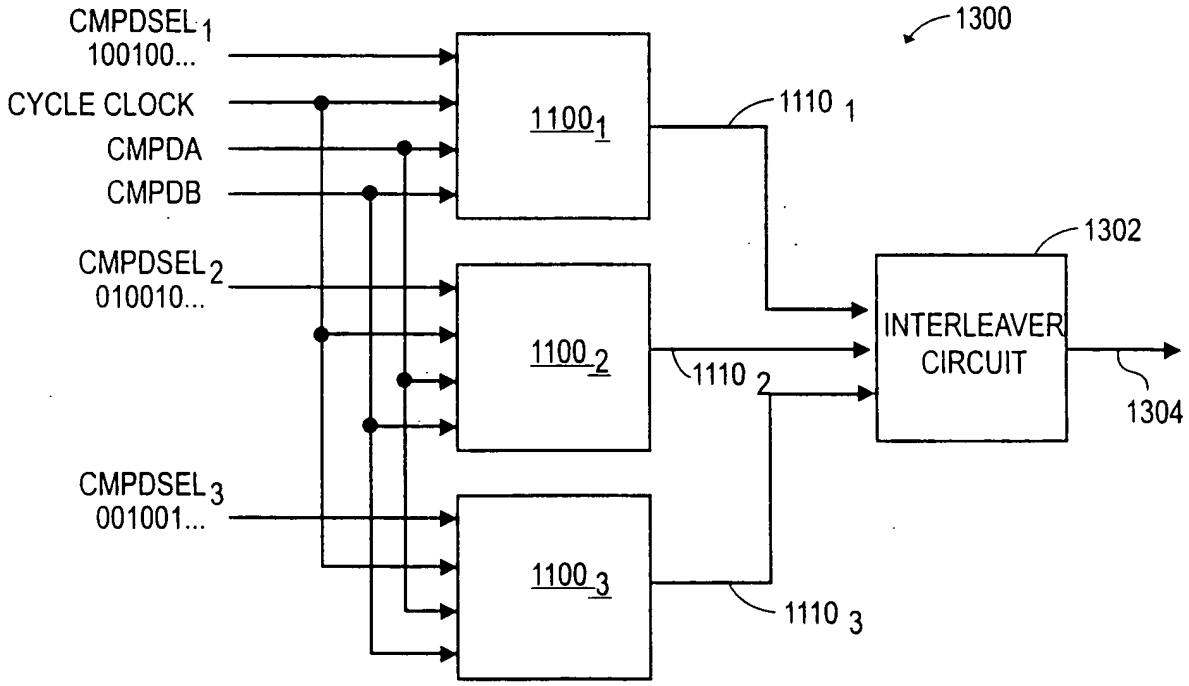
1300
CMPDSEL 1
100100...
CYCLE CLOCK
CMPDA
CMPDB
CMPDSEL 2
010010...
CMPDSEL 3
001001...
1100 1
1100 2
1100 3
1110 1
1110 2
1110 3
1302
INTERLEAVER CIRCUIT
1304

FIG. 15

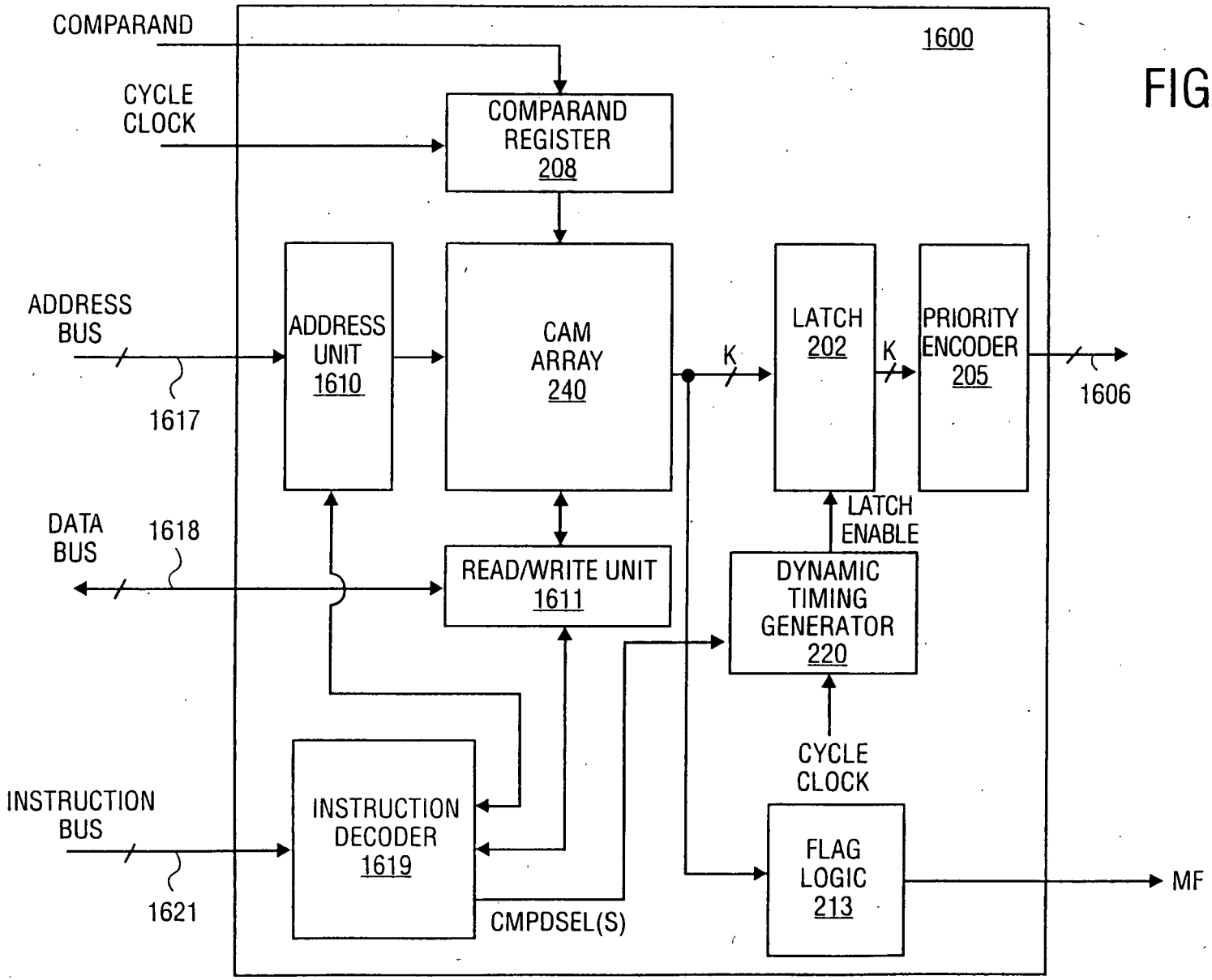
COMPARAND
1600
CYCLE CLOCK
COMPARAND REGISTER 208
ADDRESS BUS
ADDRESS UNIT 1610
CAM ARRAY 240
K
LATCH 202
K
PRIORITY ENCODER 205
1606
1617
DATA BUS
1618
READ/WRITE UNIT 1611
LATCH ENABLE
DYNAMIC TIMING GENERATOR 220
CYCLE CLOCK
INSTRUCTION BUS
INSTRUCTION DECODER 1619
FLAG LOGIC 213
MF
1621
CMPDSEL(S)

FIG. 16

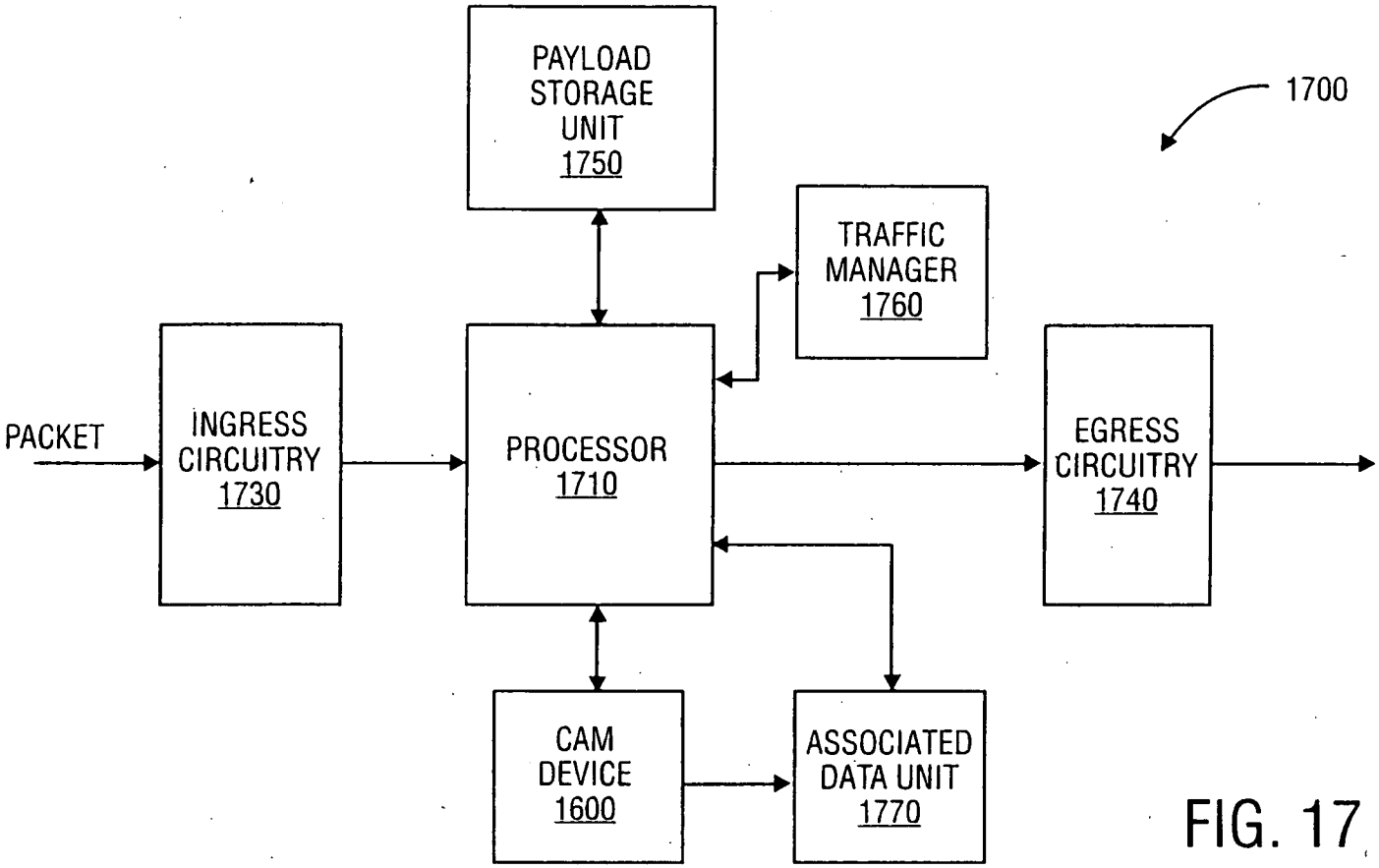
PAYLOAD STORAGE UNIT 1750
1700
TRAFFIC MANAGER 1760
PACKET
INGRESS CIRCUITRY 1730
PROCESSOR 1710
EGRESS CIRCUITRY 1740
CAM DEVICE 1600
ASSOCIATED DATA UNIT 1770

FIG. 17

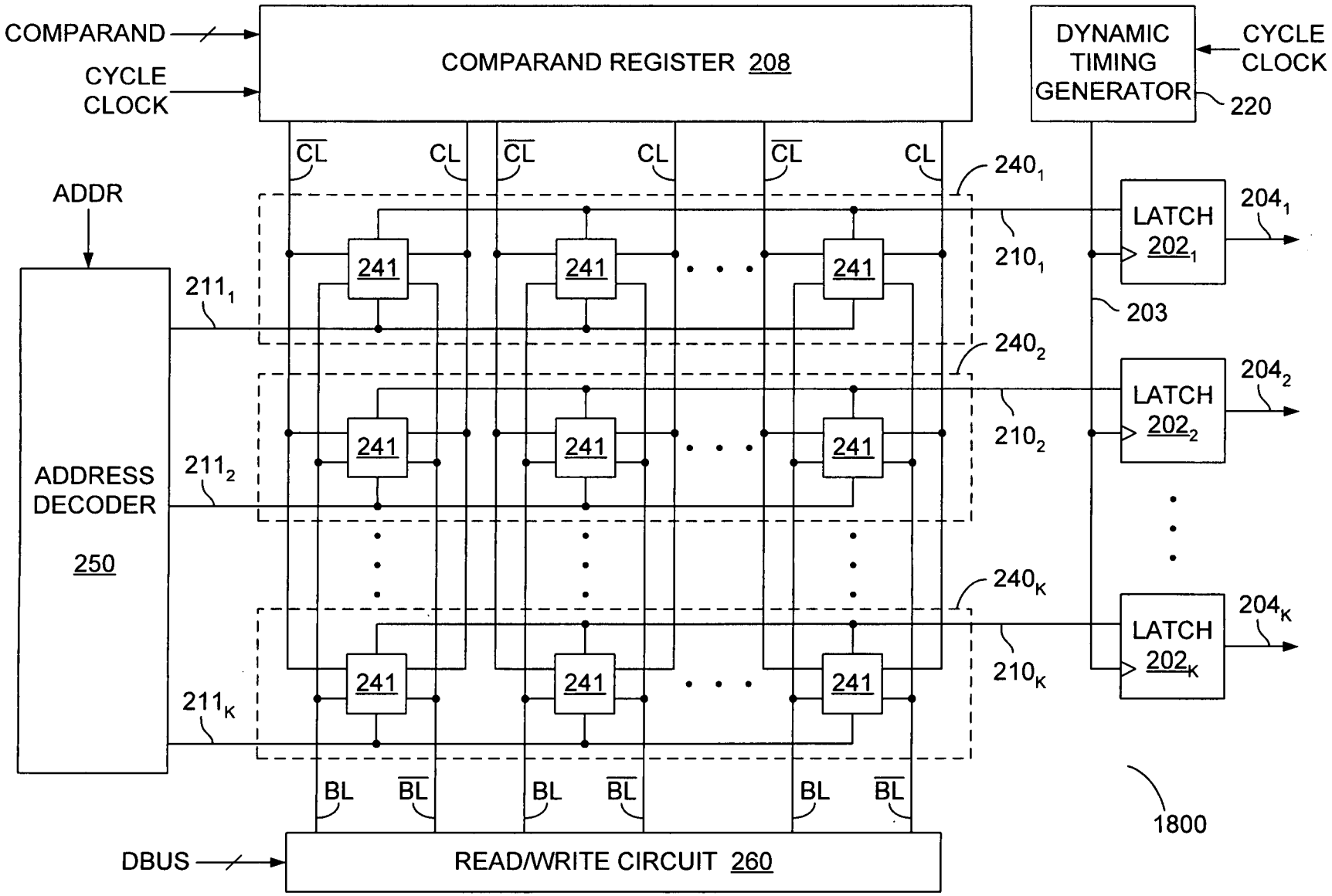
COMPARAND
CYCLE CLOCK
COMPARAND REGISTER 208
DYNAMIC TIMING GENERATOR
CYCLE CLOCK
220
ADDR
ADDRESS DECODER 250
CL
241
240$_1$
240$_2$
240$_K$
210$_1$
210$_2$
210$_K$
211$_1$
211$_2$
211$_K$
LATCH 202$_1$
LATCH 202$_2$
LATCH 202$_K$
204$_1$
204$_2$
204$_K$
203
BL
DBUS
READ/WRITE CIRCUIT 260
1800

FIG. 18

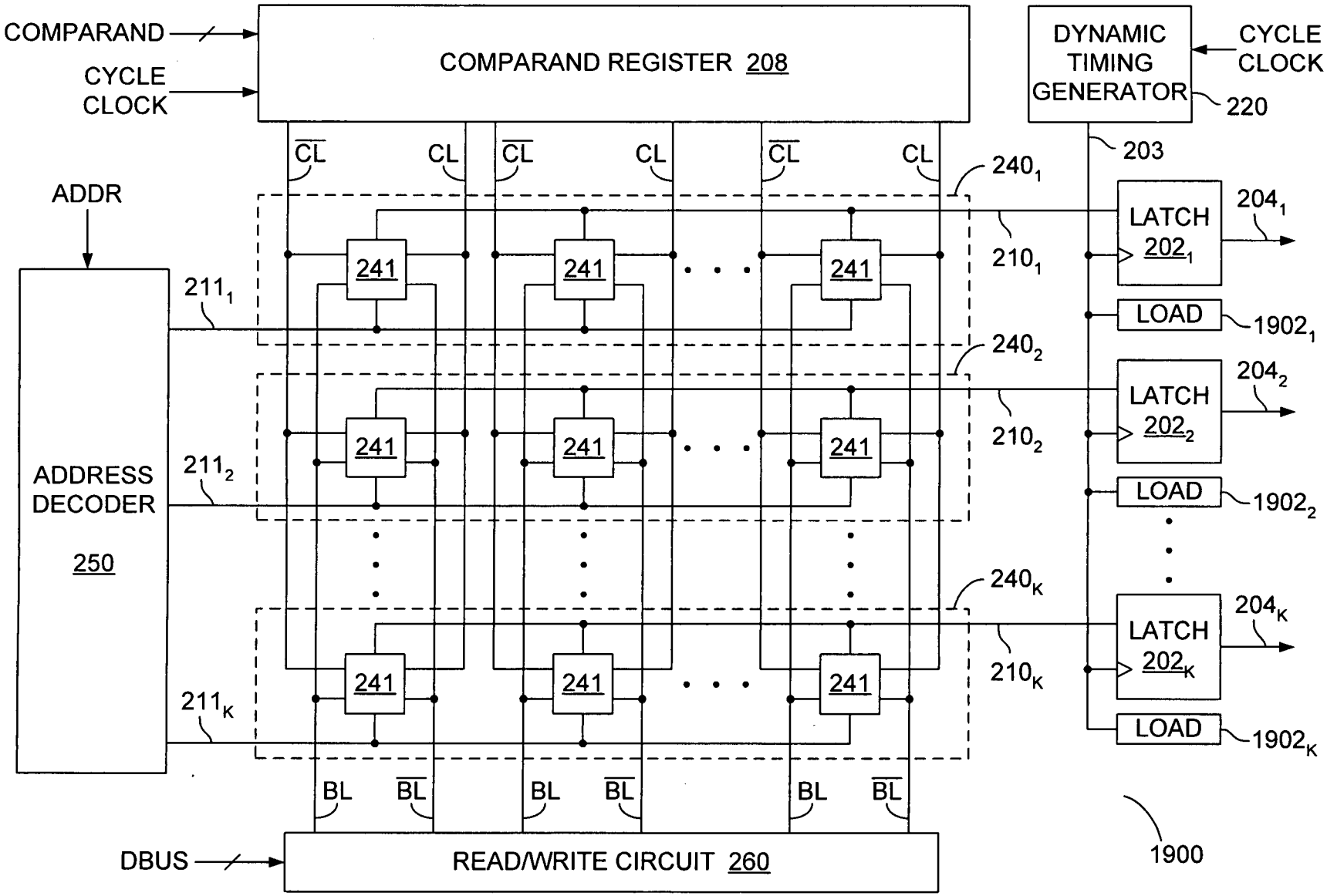
COMPARAND
CYCLE CLOCK
COMPARAND REGISTER 208
DYNAMIC TIMING GENERATOR
CYCLE CLOCK
220
203
ADDR
ADDRESS DECODER 250
CL
241
240$_1$
240$_2$
240$_K$
210$_1$
210$_2$
210$_K$
211$_1$
211$_2$
211$_K$
LATCH 202$_1$
LATCH 202$_2$
LATCH 202$_K$
204$_1$
204$_2$
204$_K$
LOAD
1902$_1$
1902$_2$
1902$_K$
BL
DBUS
READ/WRITE CIRCUIT 260
1900

FIG. 19

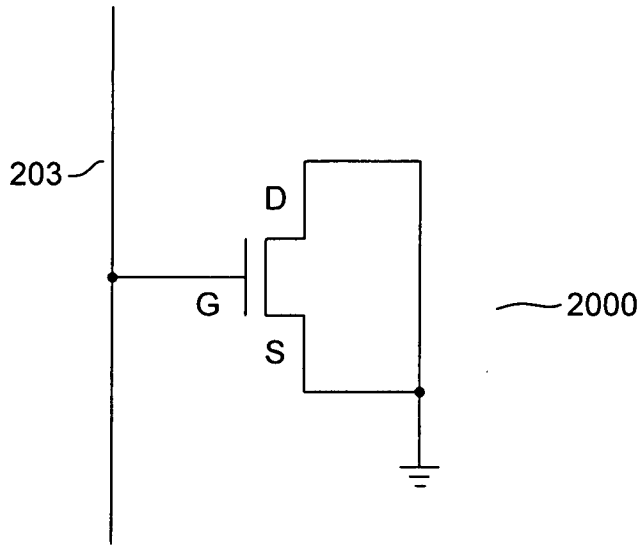

FIG. 20

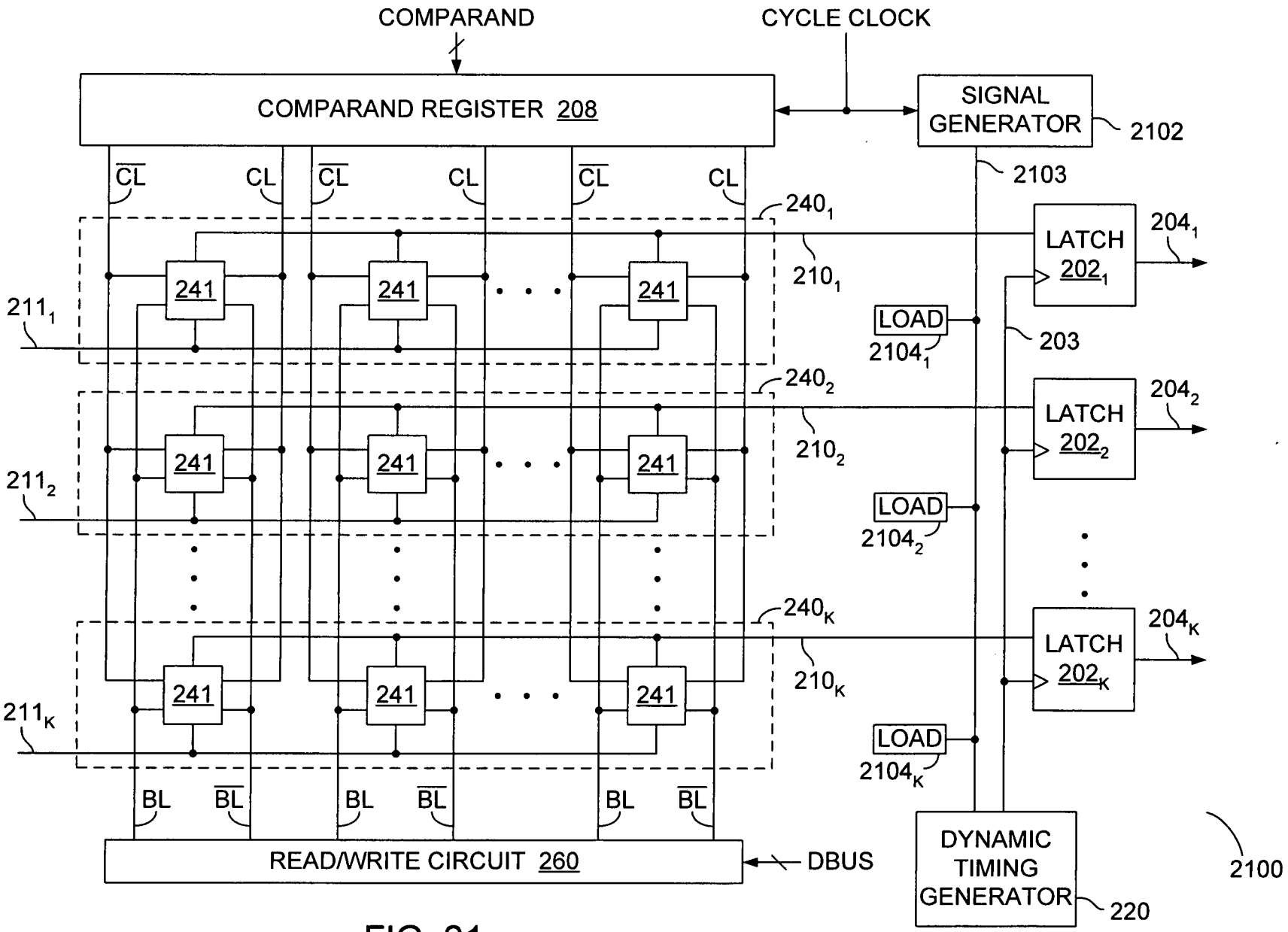
COMPARAND
CYCLE CLOCK
COMPARAND REGISTER 208
SIGNAL GENERATOR
2102
2103
CL
241
240$_1$
210$_1$
211$_1$
LATCH 202$_1$
204$_1$
LOAD 2104$_1$
203
240$_2$
210$_2$
211$_2$
LATCH 202$_2$
204$_2$
LOAD 2104$_2$
240$_K$
210$_K$
211$_K$
LATCH 202$_K$
204$_K$
LOAD 2104$_K$
BL
READ/WRITE CIRCUIT 260
DBUS
DYNAMIC TIMING GENERATOR
220
2100

FIG. 21

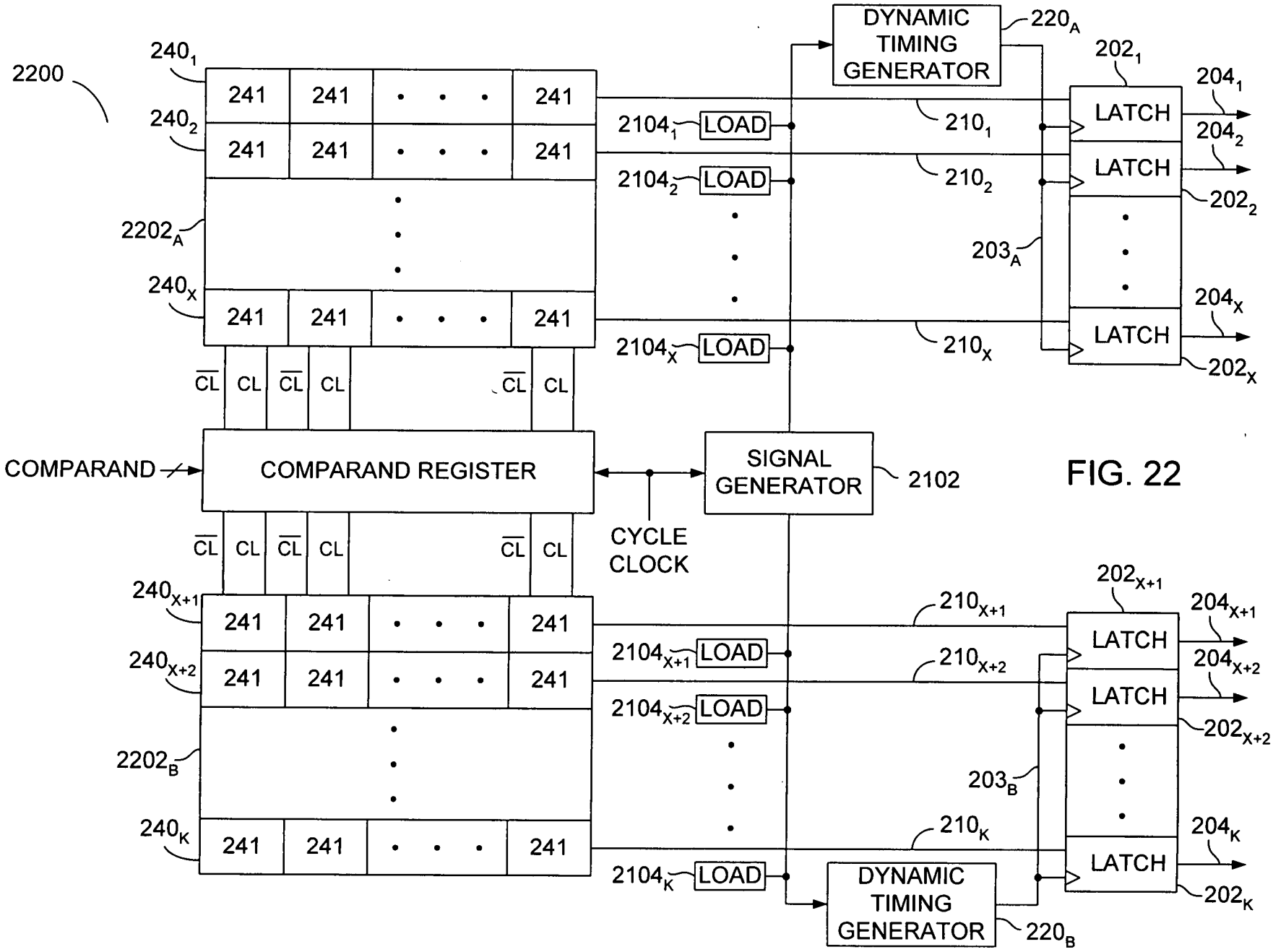
2200
240_1
240_2
2202_A
240_X
241
2104_1 LOAD
2104_2 LOAD
2104_X LOAD
DYNAMIC TIMING GENERATOR
220_A
210_1
210_2
210_X
203_A
202_1
LATCH
204_1
204_2
202_2
204_X
202_X
CL
COMPARAND
COMPARAND REGISTER
SIGNAL GENERATOR
2102
CYCLE CLOCK
240_{X+1}
240_{X+2}
2202_B
240_K
2104_{X+1} LOAD
2104_{X+2} LOAD
2104_K LOAD
210_{X+1}
210_{X+2}
210_K
203_B
202_{X+1}
204_{X+1}
204_{X+2}
202_{X+2}
204_K
202_K
DYNAMIC TIMING GENERATOR
220_B

FIG. 22